		Application/Control No.	Applicant(s)/Patent Under Reexamination
Notice of References Cited		10/674,085	FALLON ET AL.
		Examiner	Art Unit	
		Helen Rossoshek	2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0184603	12-2002	Hassibi et al.	716/2
*	B	US-6,011,911	01-2000	Ho et al.	716/5
*	C	US-6,066,180	05-2000	Kim et al.	716/19
*	D	US-6,389,582	05-2002	Valainis et al.	716/9
*	E	US-6,678,644	01-2004	Segal	703/15
*	F	US-6,367,052	04-2002	Steinberg et al.	716/2
*	G	US-4,554,625	11-1985	Otten	700/171
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	NN8712251, "Method for Improving Geometric Packaging of Circuit Chip Modules: Utilizing Top-Down Slicing-Based Floorplanning", December 1, 1987, Voll.No: 30, Issue No.: 7, Pages: 251-253
	V	Prieto et al., "A performance-driven placement algorithm with simultaneous Place&Route optimization for analog ICs", 17-20 March 1997, European Design and Test Conference, ED&TC 97, Page(s):389 - 394□□
	W	Kleinhans et al., "GORDIAN: VLSI placement by quadratic programming and slicing optimization", March 1991, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on□□Volume 10, Issue 3, Page(s):356 - 365
	X	Maruvada et al., "Placement with symmetry constraints for analog layout using red-black trees", 25-28 May 2003 Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on, Volume 5, Page(s):V-489 - V-492 vol.5

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.